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| 09/683,428 | 12/28/2001 | William H. Moody II | CROSS1510 | 1923 |

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| EXAMINER | |
|---|---|
| WANG, ALBERT C | |

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DATE MAILED: 03/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 09/683,428 | Applicant(s) MOODY, WILLIAM H. | |
|---|---|---|---|
| | Examiner Albert Wang | Art Unit 2115 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-26 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-26 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2, 4, 5, and 6.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Original claims 1-26 are pending.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1, 2, 5, 6, 8-13, 15, 16, 21, and 23 are rejected under 35 U.S.C. 102(a) as being anticipated by Mayhead et al., U.S. Patent No. 6,216,186 ("Mayhead").

As per claim 1, Mayhead discloses a method comprising:

providing a primary electronic component having a first identifier stored therein (Fig. 2; Col. 6, lines 43-55, processor 32 on motherboard 30 having memory registers 52-58);

providing a secondary electronic component having a second identifier stored therein (pluggable module 40 having registers 42-48);

coupling the secondary component to the primary component (via bus 36);

comparing the first identifier to the second identifier (Col. 5, lines 1-12; Col. 6, lines 57-62; Fig. 5, step S2);

operating the primary component in conjunction with the secondary component if the first identifier matches the second identifier (Fig. 5, step S3; Col. 8, lines 47-53); and

operating the primary component without the secondary component if the first identifier does not match the second identifier (Fig. 5, step S4; Col. 8, lines 47-53).

As per claim 2, Mayhead discloses storing the first identifier in a memory in the primary component and storing the second identifier in a memory of the secondary component (Fig. 2; Col. 6, lines 43-55).

As per claim 5, Mayhead discloses the first interconnect comprises a PCI bus (Col. 9, lines 27-40).

As per claim 6, Mayhead discloses enabling the secondary component if the first identifier matches the second identifier; and disabling the secondary component if the first identifier does not match the second identifier (Fig. 5, steps S3 and S4; Col. 8, lines 47-53).

As per claims 8 and 9, Mayhead discloses providing at least one additional electronic secondary component having an additional identifier stored therein (Fig. 6, devices 128-132).

As per claim 10, Mayhead discloses comparing the first identifier to the additional identifier (Col. 9, lines 59-67; Fig. 5, applied to additional secondary component).

As per claim 11, Mayhead discloses operating the primary component in conjunction with the additional secondary component if the first identifier matches the additional identifier (Fig. 5, steps S3 and S4; Col. 8, lines 47-53).

As per claim 12, Mayhead discloses operating the primary component without the additional secondary component if the first identifier does not match the additional identifier (Fig. 5, steps S3 and S4; Col. 8, lines 47-53).

As per claim 13, Mayhead discloses a system comprising:

a primary component having a first memory, wherein the first memory has a first identifier stored therein (Fig. 2; Col. 6, lines 43-55, processor 32 on motherboard 30 having memory registers 52-58); and

a secondary component having a second memory, wherein the second memory has a second identifier stored therein (pluggable module 40 having registers 42-48);

wherein the secondary component is configured to be coupled to the primary component (Fig. 2);

wherein the primary component is configured to compare the first identifier to the second identifier (Col. 5, lines 1-12; Col. 6, lines 57-62; Fig. 5, step S2);

wherein the primary component is configured to enable operation with the secondary component if the first identifier matches the second identifier (Fig. 5, step S3; Col. 8, lines 47-53);

wherein the primary component is configured to prevent operation with the secondary component if the first identifier does not match the second identifier (Fig. 5, step S4; Col. 8, lines 47-53).

As per claim 15, Mayhead discloses the secondary component is configured to be coupled to the primary component by a first interconnect, wherein if the primary component is enabled to operate with the secondary component, data is transferred between the primary component and the secondary component via the first interconnect during operation (Fig. 2, bus 36; Fig. 6, D-bus).

As per claim 21, Mayhead discloses an electrical component configured to have a secondary component coupled thereto (Fig. 2, motherboard 30 having pluggable module 40), wherein the electrical component comprises:

a functional portion (Col. 6, lines 43-55, processor 32);

an interface configured to couple the functional portion to a secondary component (bus 36);

a memory configured to store a first identifier (registers 52-58); and

a comparator configured to receive a second identifier from the secondary component and to compare the first identifier to the second identifier (Col. 6, lines 57-62), wherein the comparator is configured to enable operation of the functional portion with the secondary component if the first identifier matches the second identifier and to disable operation of the functional portion with the secondary component if the first identifier does not match the second identifier (Fig. 5, step S3; Col. 8, lines 47-53).

As per claims 16 and 23, since Mayhead discloses the method of claim 5, Mayhead discloses the claimed system and electrical component

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 3, 4, 14, 17, 18, 22, 25, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mayhead as applied to claims 1, 2, 13, 15, and 21 above, and further in view of Goers et al., U.S. Patent No. 6,661,236 ("Goers").

As per claim 17, Mayhead does not expressly teach a second interconnect. Goers teaches a secondary component is further configured to be coupled to a primary component by a second interconnect, wherein the primary component is configured to receive the second identifier via the second interconnect (Fig. 1; Col. 3, lines 25-35 and 51-67, pluggable electrical unit 2 with ROM 21 coupled to base unit 1 by identification bus 41).

At the time of the invention, it would have been obvious to one skilled in the art to apply Goer's second interconnects to Mayhead's system. Mayhead and Goer are analogous art since they from the same field of endeavor involving identifying compatibility between components. A motivation for doing so would have been to take advantage of the I2C protocol.

As per claim 14, Goer teaches at least one of the first and second memories comprises a non-volatile memory (Fig. 1; Col. 3, lines 51-60, ROM 21).

As per claim 18, Goer teaches the second interconnect comprises an Inter-IC (I.sup.2 C) bus (Col. 3, lines 51-67).

As per claims 3 and 4, since Mayhead/Goer teaches the system of claims 14 and 17, the combination teaches the claimed method.

As per claims 22, 25, and 26, since Mayhead/Goer teaches the system of claims 14, 17, and 18, the combination teaches the claimed electrical component.

4. Claims 7, 19, 20, 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mayhead as applied to claims 1, 13 and 21 above, and further in view of Nolan et al., U.S. Patent No. 6,214,068 ("Nolan").

As per claim 7, Mayhead does not expressly teach comparing during boot-up. Nolan teaches comparing during boot-up (Fig. 6A&B; Col. 10, lines 49-52). At the time of the invention, it would have been obvious to one skilled in the art to apply Nolan's comparing during boot-up to Mayhead's method. A motivation for doing so would have been to ensure verification of system components at boot-up.

As per claim 19, Nolan teaches a system where the primary component is comprises a storage router (Col. 3, lines 15-24).

As per claim 20, Nolan teaches the secondary component is selected from the group consisting of: a Fibre Channel interface module; an LVD SCSI interface module; an HVD SCSI module; and an iSCSI interface module (Fig. 3; Col. 4, lines 1-22).

As per claim 24, since Mayhead/Nolan teaches the system of claim 19, the combination teaches the claimed electrical component.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert Wang whose telephone number is 703-305-5385. The examiner can normally be reached on M-F (9:30 - 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 703-305-9717. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

aw
March 22, 2004

THOMAS LEE
SUPERVISORY PATENT EXAMINER
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